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TRANSMITTAL FORM (to be used for all correspondence after initial filing)	Application Number	10/605,292	
	Filing Date	9/19/03	
	First Named Inventor	HOSOKAWA, ET AL.	
	Group Art Unit	NOT ASSIGNED	
	Examiner Name	NOT ASSIGNED	
Total Number of Pages in This Submission		Attorney Docket Number	JP920020166US1

ENCLOSURES (check all that apply)		
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<input type="checkbox"/> Fee Attached	<input type="checkbox"/> Drawing(s)	<input type="checkbox"/> Appeal Communication to Board of Appeals and Interferences
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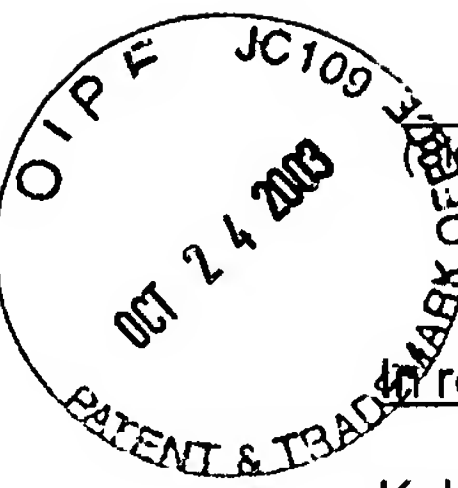
SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT	
Firm or Individual name	IRA D. BLECKER, REG. NO. 29,894
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 Judy Paolillo 10/22/03
(Signature & date)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

re application of _____:

10/22/2003

Kohji Hosokawa, et al. :

Group Art Unit: Not yet assigned

Serial No. Application of
10/605,292 :

Examiner: Not yet assigned

Filed: 9/19/03 :

International Business Machines Corporation
2070 Route 52
Hopewell Junction, NY 12533

TITLE: DRAM Circuits and its Operation Method

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to the duty of disclosure set forth in 37 C.F.R. 1.56, and further pursuant to the provisions of 37 C.F.R. 1.97 and 1.98, applicants hereby respectfully submit copies of the non-US patents and publications as listed on Form PTO-1449, attached hereto.

In citing these documents, no representation is made nor intended as to the pertinency or non-pertinency of the art, that better art than that listed is not available, or that other art is not applicable.

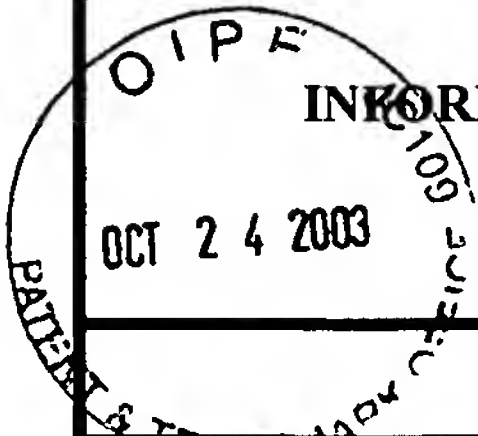
No fee is believed to be due for this submission. If any fees are required, however, the Commissioner is hereby authorized to charge such fees to Deposit Account No. 09-0458.

Respectfully submitted,
Kohji Hosokawa, et al.

By 

Ira D. Blecker, Attorney
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Telephone No. 845-894-2580

JP920020166US1



INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

Docket Number (Optional)

JP920020166US1

Application Number

10/605,292

Applicant(s)

KOHJI HOSOKAWA, ET AL.

Filing Date

9/19/03

Group Art Unit

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

FOREIGN PATENT DOCUMENTS

	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
							YES	NO
		07-094597	07.04.95	JAPAN				
		2001-168300	22.06.01	JAPAN				
		02-183489	18.07.90	JAPAN				
		04-094569	26.03.92	JAPAN				

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

		Article: IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 34, NO. 6, JUNE 1999 "MULTIPLE TWISTED DATALINE TECHNIQUES FOR MULTIGIGABIT DRAMS'S", by Dong-Sun Min, pp. 856-865
		Article in ISSCC 2002 Digest of Technical Papers, Sessin 9, 9.3 "A 300MHz Multi-banked eDRAM Macro Featuring GND Sense, Bit-Line Twisting and Direct Reference Cell Write" by John Barth, Darren Anand, Jeff Dreibelbis, Erik Nelson pp. 156-157

EXAMINER

DATE CONSIDERED

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